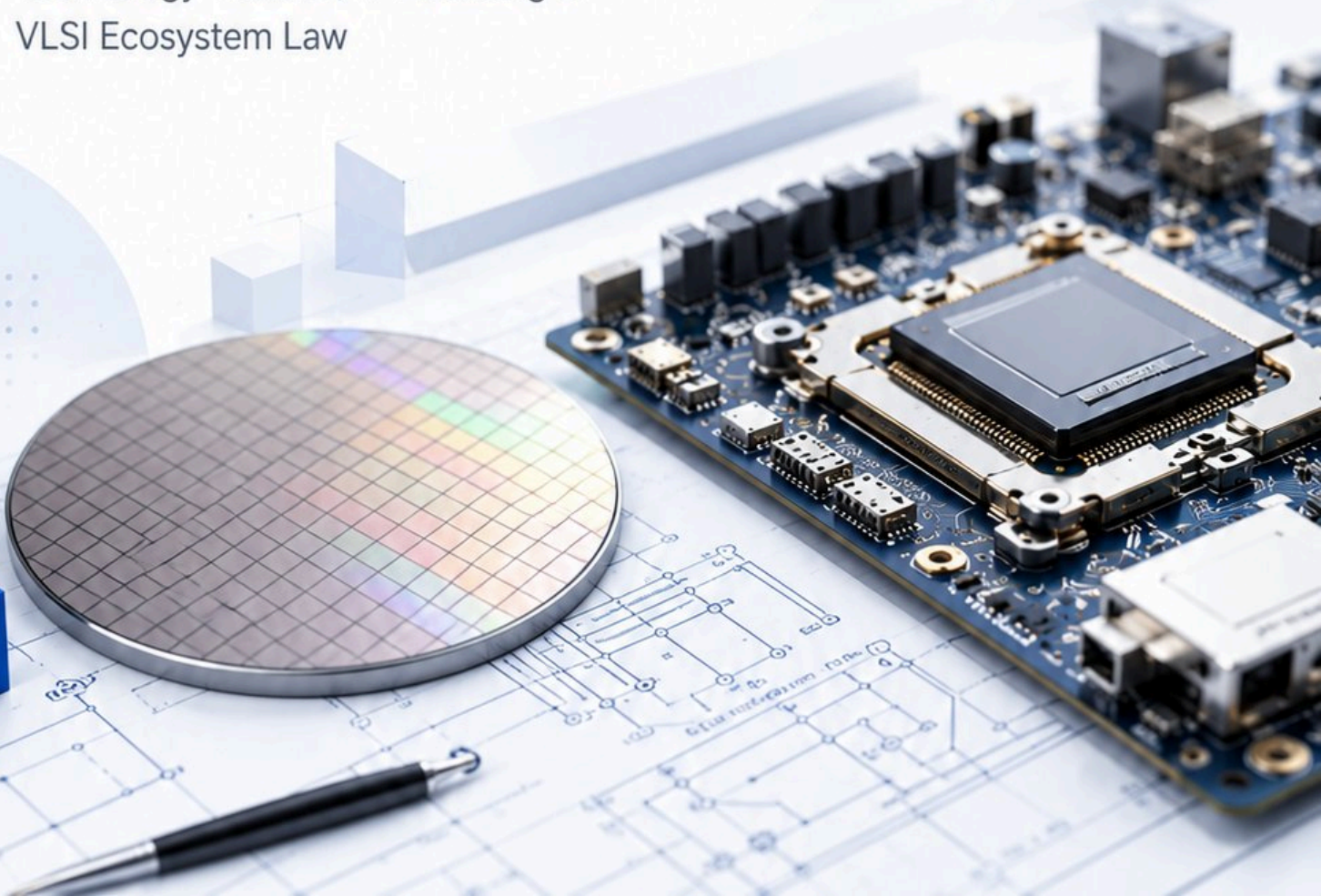


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Semiconductor & Advanced Electronics: Legal & Investment Framework

SeMI Scheme, Chip Design PLI,
Technology Transfer, IP Licensing &
VLSI Ecosystem Law



Semiconductor & Advanced Electronics: Legal & Investment Framework

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CHAPTER ONE

India Semiconductor Mission and the SeMI Scheme

Rs. 76,000 Crore Programme, Fab Incentives, ATMP Support, Compound Semiconductors and the ISM Architecture

India's semiconductor ambition — crystallised in the India Semiconductor Mission and its associated incentive schemes — represents the most strategically ambitious industrial policy initiative in the country's post-liberalisation history. Understanding the legal architecture of these schemes is essential for any counsel advising semiconductor manufacturers, technology investors, or government agencies involved in this sector.

1.1 India Semiconductor Mission: Rationale and Architecture

The India Semiconductor Mission (ISM), established under the Semiconductor and Display Fab Ecosystem Programme approved by the Cabinet in December 2021 with a budgetary outlay of Rs. 76,000 crore, is designed to create a comprehensive domestic semiconductor manufacturing ecosystem encompassing fabrication (fab) for logic and memory chips, assembly, testing, marking, and packaging (ATMP), compound semiconductor manufacturing, and semiconductor chip design. The strategic imperative driving the ISM is India's near-total dependence on imported semiconductors — India imports approximately USD 20 billion of semiconductors

annually, a figure projected to grow to USD 100+ billion by 2030 as electronics consumption expands, and the absence of domestic semiconductor manufacturing creates a critical strategic vulnerability in an increasingly digital economy. The global semiconductor supply chain disruptions of 2020–2022, which caused widespread shortages of chips for automotive, consumer electronics, and industrial applications, dramatically illustrated the economic and strategic consequences of over-concentration of semiconductor manufacturing in a small number of facilities primarily in Taiwan and South Korea, accelerating government and industry interest in supply chain diversification through new fab investments in the United States (CHIPS Act), Europe (EU Chips Act), Japan, and India.

ISM is administered by a dedicated government entity, the India Semiconductor Mission (ISM) SPV, under the Department for Promotion of Industry and Internal Trade (DPIIT) with oversight from MEITY. The ISM provides fiscal support to semiconductor manufacturing projects through the Scheme for Setting up of Semiconductor Fabs in India (commonly referred to as the "SeMI scheme") and the Scheme for Setting up of Compound Semiconductors/Silicon Photonics/Sensors (Fab) and Semiconductor Atmel (ATMP/OSAT) Facilities in India. The legal basis for ISM and its associated incentive schemes is the Cabinet approval of December 2021, supplemented by scheme-specific guidelines notified by MEITY that specify eligibility criteria, the fiscal support framework, the application and approval process, and the conditions of the support agreement between the government and the approved project proponent. The ISM approval process involves: submission of a detailed project proposal by the prospective fab or ATMP developer; technical and financial evaluation by ISM's expert committee; negotiation of the support agreement terms; Cabinet approval (for projects above specified financial thresholds); and execution of the formal support agreement that creates the legally binding framework for the government-industry partnership.

1.2 Semiconductor Fab Incentives: 50% Fiscal Support

The Scheme for Setting up of Semiconductor Fabs in India provides fiscal support equivalent to 50% of the project cost for eligible semiconductor fabrication facilities, disbursed in tranches linked to verified construction and equipment installation milestones. This is an extraordinary level of government support — comparable to the incentive rates offered under the US CHIPS Act (which provides up to 35% investment tax credit plus direct grants) and the EU Chips Act — and reflects the Indian government's recognition that semiconductor fab economics are not commercially viable without substantial government co-investment, given the enormous capital requirement (USD 3–10 billion for a leading-edge fab), the 5–7 year development timeline, and the uncertainty about demand during the extended development period. The 50% fiscal support is a direct grant to the project company, not a tax credit or incentive linked to future production — it provides real cash support for construction, equipment procurement, and infrastructure development. The conditions attached to the fiscal support agreement include: minimum

investment commitment by the project proponent (the remaining 50% of project cost plus working capital); technology commitment (specifying the minimum technology node or process capability); localisation and indigenisation requirements (progressively increasing the domestic sourcing of materials and equipment); employment generation targets; and commercial production timelines. Non-achievement of the agreed milestones can result in clawback of disbursed support at interest, creating significant financial exposure for project proponents who fail to deliver on their commitments.

1.3 ATMP and Compound Semiconductor Incentives

For semiconductor Assembly, Testing, Marking, and Packaging (ATMP) and Outsourced Semiconductor Assembly and Test (OSAT) facilities — which represent a less capital-intensive (USD 200 million to USD 1 billion per facility) but strategically important segment of the semiconductor value chain — the government provides fiscal support of 50% of capital expenditure under the compound semiconductor and ATMP scheme. India's first approved fab investment, Micron Technology's USD 825 million ATMP facility in Sanand, Gujarat (announced in June 2023), will process DRAM and NAND flash memory chips for the global semiconductor market, benefiting from the 50% ATMP support. The Tata Electronics-Powerchip Semiconductor Manufacturing Corporation (PSMC) fab project in Dholera, Gujarat — India's first greenfield semiconductor fab, announced in February 2024 — will manufacture chips at 28nm and above nodes for power management, display driver, and microcontroller applications, with a planned investment of approximately Rs. 91,000 crore and fiscal support from the ISM scheme. These pioneering projects will establish India's semiconductor manufacturing credentials and create the ecosystem infrastructure — trained workforce, supply chains, logistics, and regulatory experience — needed for subsequent, more advanced investments.

Design Linked Incentive: Chip Design PLI Architecture

DLI Scheme, Expenditure Reimbursement, Deployment Incentive, IP Creation and the India Chip Design Ecosystem

2.1 Design Linked Incentive Scheme: Overview

The Design Linked Incentive (DLI) scheme, notified as part of the December 2021 semiconductor package with a total outlay of Rs. 7,500 crore over six years, provides financial support specifically for semiconductor chip design companies — fabless design companies, integrated device manufacturers (IDMs) with India design operations, and academic institutions conducting semiconductor research — to develop India-origin chip designs for commercial production. Unlike the fab incentives (which support capital-intensive manufacturing), the DLI targets the intellectual property creation side of the semiconductor value chain — designing the chips that fabs will eventually manufacture. India has a large and globally respected semiconductor design talent pool: tens of thousands of VLSI design engineers work in India, predominantly for the India design centres of global semiconductor companies (Qualcomm, Intel, MediaTek, Texas Instruments, Analog Devices, NXP, Infineon, and others). The DLI scheme aims to catalyse the development of India-headquartered chip design companies that own the IP of the chips they design — as opposed to the service model of existing India design centres, which design chips owned by their overseas parent companies.

2.2 DLI Financial Incentives: Expenditure Reimbursement and Deployment

The DLI scheme provides two categories of financial support: a product design incentive (reimbursement of 50% of eligible expenditure, subject to a maximum of Rs. 15 crore per applicant per year for up to three years) for the design and development costs of new chip designs; and a deployment linked incentive (6% of net sales of chips incorporating India-designed IP, for five years after commercial deployment, subject to annual and aggregate caps) that rewards the commercial success of DLI-supported designs. The product design incentive covers: EDA (Electronic Design Automation) tool licence fees; semiconductor IP licence fees (for third-party IP blocks incorporated in the design); prototype and tape-out costs (the cost of fabricating test wafers at an external fab to verify the design); testing and characterisation costs; and human resource costs (salary of the design team working on the DLI-supported project). The combination of upfront expenditure reimbursement (reducing the financial risk of design investment) and backend deployment incentive (rewarding commercial success) creates a financial model that is appropriate for semiconductor chip design, where the upfront investment in a new chip design is 3–5 years of engineering effort and millions of dollars of tool and IP

licence costs, and commercial returns are realised only if and when the design achieves volume production — a high-risk, high-reward profile that government support can meaningfully de-risk.

2.3 IP Ownership and DLI Compliance

A critical condition of DLI participation is that the supported company must own the IP of the chip design it develops with DLI support — the government's support is intended to build India's intellectual property base in semiconductor design, not to subsidise the development of IP that will be owned by overseas parent companies or transferred to foreign entities. DLI scheme guidelines require: that the chip design IP is registered in India or at minimum is owned by an Indian-incorporated entity; that any third-party IP (EDA tool outputs, licensed IP blocks) incorporated in the design does not compromise the Indian entity's ownership of the overall design; and that the DLI-supported design is not transferred, assigned, or exclusively licensed to a foreign entity during the support period or for a specified post-support period, without MEITY's consent. For chip design companies with complex global IP structures — where design teams in India create chip designs that are nominally owned by IP holding companies in Singapore, the Netherlands, or the United States — the DLI's India IP ownership requirement creates a structural compliance challenge that must be addressed through IP restructuring before the DLI application is submitted. Legal practitioners with expertise in both Indian IP law and international IP structuring are therefore essential advisors for companies seeking to participate in the DLI programme.

Technology Transfer and Licensing in Semiconductors

Patent Act 1970, FEMA Royalty Provisions, Process IP Licensing, EDA Agreements and Trade Secret Protection

3.1 Legal Framework for Technology Transfer

Semiconductor technology transfer — the conveyance of process technology, design methodology, manufacturing know-how, and associated intellectual property from a technology licensor to an Indian recipient — is governed by a combination of Indian IP law and regulatory frameworks. The Patents Act, 1970 governs the protection and licensing of patented semiconductor inventions, including process patents (for manufacturing processes such as specific deposition, etch, and lithography techniques) and device patents (for novel semiconductor device structures). The Copyright Act, 1957 governs the protection of software code used in semiconductor design tools and embedded software. The Designs Act, 2000 protects the aesthetic design of semiconductor package layouts. Trade secrets — the most commercially important category of semiconductor know-how, encompassing process recipes, yield optimisation techniques, and design methodologies that may not be patented for competitive secrecy reasons — are protected under the general confidentiality and misappropriation principles of the Indian Contract Act, 1872 and the tort of breach of confidence, without the benefit of a dedicated trade secrets statute (India does not yet have a standalone trade secrets law comparable to the US Defend Trade Secrets Act or the EU Trade Secrets Directive). FEMA regulations (specifically the Master Direction on Transfer of Technology Abroad) govern the cross-border payment of royalties and technical service fees for technology licences — requiring automatic route reporting to the Reserve Bank of India for royalty payments that meet specified parameters, and prior approval for royalties that exceed permitted limits or are structured in ways that trigger FEMA reporting obligations.

3.2 EDA Tool Licensing: Commercial and Legal Dimensions

Electronic Design Automation (EDA) tools — the specialised software used for semiconductor circuit design, physical layout, timing analysis, simulation, and verification — are licensed by a handful of dominant global providers (Cadence Design Systems, Synopsys, Siemens EDA/Mentor Graphics) under complex multi-year licence agreements that are among the most commercially significant IP licences in the semiconductor industry. For India's chip design community — both the captive design centres of global semiconductor companies and the emerging independent fabless design companies supported by the DLI scheme — EDA tool licence agreements govern access to the core development infrastructure without which chip design is impossible. The legal

terms of EDA licence agreements that Indian companies must navigate include: geographic scope (whether the licence permits use only in India, in specific countries, or globally); user seat restrictions (whether the licence covers a fixed number of concurrent users or all users of the licensee); node restrictions (whether the licence covers design tools for all semiconductor process nodes or is restricted to specific nodes as determined by the fab's process design kit (PDK) compatibility); and export control restrictions (many EDA tools are export-controlled under the US EAR, and EDA licence agreements typically include provisions requiring licensees to comply with US export control regulations, which may restrict the tools' use by employees who are nationals of certain countries or who work on programmes with military applications). For Indian chip design companies, understanding and complying with the export control provisions of their EDA licence agreements is a non-trivial compliance obligation that requires regular training for design teams and careful management of the nationalities and assignments of personnel who access EDA tools.

VLSI Ecosystem: Legal Framework and Investment Structuring

Approved Fab Projects, SEZ Legal Framework, Employment Law and US-India Technology Control Coordination

4.1 Approved Semiconductor Projects: Legal Status

The approved semiconductor fab and ATMP projects under the ISM — Micron's ATMP facility in Sanand (Gujarat), Tata Electronics-PSMC's fab in Dholera (Gujarat), and CG Power and Industrial Solutions-Renesas Electronics-Stars Microelectronics' ATMP facility in Sanand (Gujarat) — each involve complex legal structures spanning: the project company's incorporation and shareholding structure; the fiscal support agreement with the ISM SPV specifying the government's financial commitments and the project proponent's obligations; the land and infrastructure arrangements with the state government host (Gujarat's industrial development infrastructure); the technology licence or joint venture agreement with the technology partner (PSMC for Tata Electronics, Renesas and Stars Microelectronics for CG Power); the EPC (Engineering, Procurement, and Construction) contract for the facility; and the offtake or customer agreements for the chip output. Each of these legal relationships involves provisions that must be coordinated with the others — in particular, the technology licence terms (especially IP ownership, exclusivity, and sublicensing rights) must be consistent with the ISM support agreement's IP ownership requirements, and the government's fiscal support disbursement conditions must align with the construction and equipment installation milestones in the EPC contract.

4.2 Export Control Coordination: US EAR and India

Semiconductor manufacturing technology — including fab process technology, ATMP equipment, and advanced chip design tools — is heavily export-controlled under the US Export Administration Regulations (EAR) administered by the Bureau of Industry and Security (BIS-US). The US government has progressively tightened export controls on advanced semiconductor technology since 2019, with the most significant restrictions implemented in October 2022 targeting: advanced logic chips (below 16nm or 14nm process nodes); advanced semiconductor manufacturing equipment; and the export of US-origin technology (including EDA tools, materials, and equipment) to designated entities. India, as a member of the Missile Technology Control Regime (MTCR), the Wassenaar Arrangement, and the Australia Group, and as a signatory of the US-India Initiative on Critical and Emerging Technology (iCET), has been designated as a "Country Group A5" partner under the US EAR — a favourable designation that simplifies US government export licensing for advanced technology to India and distinguishes

India from more restricted categories. However, Indian semiconductor companies and fab projects must still comply with US EAR requirements for any technology they receive from US entities, including compliance with the "foreign persons" restrictions that apply to certain controlled technologies regardless of geographic location.

Investment Approvals, Environmental Clearances and Fab Project Law

DPIIT Single-Window, State Incentives, Environmental Compliance for Fabs, and Project Finance Framework

5.1 Single-Window Clearance for Semiconductor Projects

Large semiconductor fab and ATMP projects require multiple regulatory clearances from both central government bodies and state government agencies, creating a complex multi-agency approval process that can add years to the project development timeline if not managed proactively. DPIIT's PM GatiShakti National Master Plan framework and the National Industrial Corridor Development Corporation (NICDC) provide central coordination for infrastructure development in designated industrial corridors (including the Dholera Special Investment Region in Gujarat, which is the designated location for India's first greenfield fab). At the state level, Gujarat's semiconductor project approvals process involves: the Gujarat Large Scale Industries Division (for industrial licence and land); the Gujarat Pollution Control Board (for environmental consent to establish and consent to operate); the State Environment Impact Assessment Authority (for Environmental Clearance for projects above specified investment thresholds); the Gujarat Electricity Regulatory Commission (for special industrial tariff arrangements for the fab's power supply); and the Gujarat Infrastructure Development Board (for infrastructure connection and utility supply agreements). Navigating this multi-agency approval process — maintaining consistent project specifications across all agency submissions, coordinating the sequencing of approvals to avoid bottlenecks, and building relationships with key government stakeholders — requires experienced project development counsel with specific knowledge of the Gujarat regulatory environment and the semiconductor sector's specific requirements.

5.2 Environmental Compliance for Semiconductor Fabs

Semiconductor fabrication facilities are among the most environmentally intensive manufacturing operations, using large volumes of ultra-pure water, toxic process chemicals (acids, solvents, fluorine compounds, dopant materials), and specialty gases (silane, phosphine, arsine), and generating significant quantities of chemical waste, effluent, and solid waste that require specialised treatment. The environmental compliance framework for Indian semiconductor fabs includes: Environmental Clearance from the Ministry of Environment, Forest and Climate Change (for projects above Rs. 500 crore investment, which covers virtually all fab projects); Consent to Establish and Consent to Operate from the State Pollution Control Board; Hazardous Waste authorisation under the Hazardous and Other Wastes Rules, 2016; and specific approvals for the ultra-pure water treatment system, chemical storage facilities, and

effluent treatment plant. The Environmental Impact Assessment (EIA) for a greenfield fab is a complex exercise requiring: assessment of the facility's chemical use and emissions; a dispersion modelling study for air emissions; a groundwater impact assessment for chemical spills; a social impact assessment for surrounding communities; and a public consultation process. International semiconductor manufacturers who have developed fabs in other countries may find that India's EIA requirements are broadly comparable to those in Europe and the United States, but that the specific standards, measurement methodologies, and administrative procedures differ significantly, requiring adaptation of their global environmental management systems to the Indian regulatory context.

Booklet IV Key Takeaways: India's semiconductor investment framework — anchored by the ISM's Rs. 76,000 crore programme providing 50% fiscal support for fabs and ATMP, and the DLI's Rs. 7,500 crore scheme supporting chip design companies — represents an unprecedented government commitment to building a domestic semiconductor ecosystem. Legal practitioners advising semiconductor investors must master the complex technology transfer, IP ownership, and export control dimensions of these investments; navigate the multi-agency approval process for fab facilities; and structure project finance arrangements that accommodate the long development timelines and the government's milestone-linked disbursement framework. The US-India iCET partnership and India's favourable EAR country group designation create a supportive technology transfer environment that is progressively enabling more advanced technology to flow to Indian semiconductor projects.

Semiconductor Law: Investment, IP and Ecosystem Development

Fab Project Legal Structures, Employee IP, VLSI Design Patents, Critical Mineral Supply Chain and Global SEZ Comparison

D.1 Fab Project Legal Structures: SPV and JV Frameworks

Semiconductor fabrication projects — characterised by their enormous capital requirements (USD 3-10 billion for a mainstream logic fab), long development timelines (4-6 years from groundbreaking to first wafer output), and complex technology and market dependencies — require carefully crafted legal structures that align the interests of the technology partner, the equity investors, the Indian government, and the project's eventual customers. The typical legal structure for an India semiconductor fab project involves: a Special Purpose Vehicle (SPV) incorporated under the Companies Act, 2013 as a joint venture between the Indian project promoter and the technology partner (holding equity in the proportion agreed in the JV agreement); the ISM fiscal support agreement between the SPV and the government (specifying the 50% fiscal support disbursement conditions); the technology licence agreement between the SPV and the technology partner (governing the use of process technology IP in the fab); a construction/EPC contract for the fab building and infrastructure; equipment purchase or lease agreements for the manufacturing tools; and customer supply agreements for the chip output. The JV agreement between the Indian promoter and the technology partner — which governs shareholder rights, board composition, management authority, reserved matters requiring consent, exit rights, and IP transfer on exit — is the most legally complex and commercially critical document in the entire project structure, since it determines the long-term control of the fab's operations and the terms on which the Indian party can continue operating the facility if the technology partner exits.

The technology licence agreement for a semiconductor fab is the most technically complex IP licence in any manufacturing sector, covering: the process technology licence (right to use the technology partner's process design rules, process flow specifications, and process integration IP to manufacture chips in the fab); equipment configuration and operational parameters (the specific settings for each piece of fab equipment that are optimised for the licensed process); yield optimisation know-how (the accumulated manufacturing intelligence about defect prevention, process control, and equipment maintenance that enables the fab to achieve commercially viable yields); and process improvement rights (the right to implement improvements to the licensed process developed by either party, and the IP ownership of such improvements). The process IP licence is non-exclusive (the technology partner retains the right to license the same technology to other fabs globally), and the licensee's right to use the

technology is typically limited to the specific fab described in the licence agreement (the Indian fab cannot use the licensed technology at other manufacturing locations without a separate licence). The royalty structure for fab technology licences typically involves: an upfront licence fee (compensating the licensor for the one-time cost of technology transfer and initial support); and a running royalty (a percentage of net sales of chips manufactured using the licensed technology), sometimes with a minimum royalty floor that provides the licensor with revenue certainty even if the fab's early commercial ramp is slower than projected.

D.2 Employee IP in Semiconductor Design: Indian Legal Framework

In semiconductor design companies — whether domestic Indian chip design startups or the India design centres of global semiconductor brands — the intellectual property created by engineers and scientists in the course of their employment is the company's most valuable asset. The legal framework governing employee-created IP in India is established by Section 17 of the Patents Act, 1970, which vests the ownership of inventions made by an employee in the employer where: the invention was made in the course of the employee's duties; the invention was made with the assistance of the employer's facilities or information; or the employee was specifically engaged to make inventions of the relevant type. Section 17 represents the default rule for patent ownership in employment contexts, but it can be modified by contract — employment agreements in semiconductor companies typically contain comprehensive IP assignment clauses that: assign to the company all inventions, discoveries, and IP created by the employee during the term of employment, whether or not related to the company's current business, and whether or not made during working hours; require the employee to promptly disclose all inventions to the company; and obligate the employee to execute all documents and provide all assistance the company requires to apply for, prosecute, and maintain patents on the assigned inventions. For semiconductor design companies, ensuring that these IP assignment obligations are clearly articulated in every employee's employment agreement — with no exceptions for inventions created "on the employee's own time" or for inventions "unrelated to the company's business" — is a fundamental IP protection measure.

D.3 Critical Minerals for Semiconductors: India's Supply Chain Strategy

Semiconductor manufacturing requires a range of critical minerals and specialty materials that are essential inputs for the fabrication process: silicon (the primary substrate material), germanium, gallium, and indium (compound semiconductor materials); rare earth elements (for specific dopant and thin film applications); and specialty chemicals including hydrofluoric acid, sulfuric acid, hydrogen peroxide, and ultra-pure water (for cleaning and etching processes). India's Critical Minerals Mission — launched in 2023 with a mandate to develop domestic critical mineral supply chains and to secure overseas supply through bilateral agreements with mineral-rich countries — identifies minerals relevant to semiconductor manufacturing as priority targets for supply chain development. The Ministry of Mines has identified lithium, cobalt, nickel,

graphite, rare earth elements, silicon, and several others as critical minerals for which India needs strategic supply security, and is pursuing: geological surveys of domestic deposits; fast-track mining licence processing for critical mineral projects; bilateral strategic mineral supply agreements with Australia, Argentina, Chile, South Africa, and the Democratic Republic of Congo; and investment in mineral processing and refining capacity that adds value to imported mineral concentrates before their use in manufacturing. For semiconductor investors considering India fabs, the development of India's critical mineral supply chain is an important enabling condition for long-term supply cost predictability and supply security — particularly for specialty gases and process chemicals that are currently entirely imported and whose supply could be disrupted by geopolitical events or export control actions by supplying countries.

D.4 US Export Controls and India's Technology Access

The US Bureau of Industry and Security's (BIS-US) Export Administration Regulations (EAR) control the export of US-origin semiconductor technology, equipment, and products — including EDA tools, semiconductor manufacturing equipment, and advanced chips — based on a classification system that assigns each controlled item an Export Control Classification Number (ECCN) specifying the control list on which it appears and the country and end-use conditions applicable to its export. India's designation as a Country Group A5 (a strategic trade partner designation established in 2023 that aligns India with the most permissive export control treatment, comparable to close US allies) significantly simplifies the export licence requirements for most dual-use items exported from the US to India. However, the October 2022 "Chip Rules" — which imposed stringent restrictions on the export of advanced semiconductor technology to China — have created compliance complexities for India's semiconductor sector where Chinese-owned entities, Chinese nationals, or Chinese-connected supply chains are involved: the "entity list" and "restricted party" screening of all transactions involving advanced semiconductor technology requires semiconductor companies operating in India to implement robust export compliance programmes that screen their employees, suppliers, customers, and technology recipients against US government restricted party lists, even for transactions that do not technically require a US export licence. The US government's willingness to provide India with access to advanced semiconductor technology — reflected in the iCET (India-US Initiative on Critical and Emerging Technology) commitments and in the CHIPS Act's prohibition on recipients of US fab incentives from using those incentives to expand China operations — creates a strategic advantage for India-based semiconductor investors that must be managed within the framework of US export control compliance.

Booklet IV — Complete Summary: India's semiconductor legal framework — spanning the ISM's Rs. 76,000 crore programme, the DLI's support for chip design IP creation, the complex technology licence and JV structures for fab projects, US export control coordination, and the Critical Minerals Mission — represents the most sophisticated technology industrial policy

framework in India's post-independence history. Legal practitioners advising semiconductor sector investors require specialised expertise in IP licensing, project finance, investment regulation, export controls, and environmental compliance to provide commercially effective counsel. The transformation of India into a significant semiconductor manufacturing and design location — which the current policy framework is designed to achieve — will create a generation of landmark legal transactions in IP licensing, joint ventures, and project finance that will define the Indian technology sector's legal landscape for decades.